#9 Translation 12/24/02

VERIFICATION OF TRANSLATION

I, the below named translator, hereby declare:

that my name and my post office address are as stated below; and

that I am knowledgeable in the English and Korean languages and that I believe the following is a true and complete translation into the English language of Korean Patent Application No. 2000-0037007 filed in the Korean Patent Office on June 30, 2000 for Letters Patent, including a true translation of the Official Certificate of the Application.

Signed this 17th day of December, 2002

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【Abstract】

The present invention relates to a method of fabricating a capacitor. The method for fabricating a high dielectric capacitor, comprising the steps of: forming an insulating layer and an antireflection layer over a semiconductor substrate on which a conductive layer is formed; forming a first contact hole by patterning the antireflection layer and the insulating layer, and forming a plug in the contact hole; removing a portion of the plug, forming a metal silicide and a barrier metal layer on the remaining plug; removing a portion of the barrier metal layer in the contact hole and forming a seed layer on the remaining seed layer; forming a dummy oxide layer over the semiconductor substrate, pattering the dummy oxide layer to form a second contact hole exposing the seed layer in the contact hole, and forming a lower electrode in the second contact hole; and removing the dummy oxide layer and forming a dielectric layer and an upper electrode.

【Selected Drawing】

Fig. 4

【Index words】

high dielectric material, oxidation, barrier metal layer, seed metal layer, misalign

【Specification】

【Title of the Invention】

METHOD OF MANUFACTURING A CAPACITOR INCLUDING A HIGH DIELECTRIC LAYER

【Brief Description of the Drawings】

Figs. 1 to 9 are cross sectional view showing a method for fabricating a semiconductor memory device according to an embodiment of the present invention.

*Description of the Principal Reference Numerals

1: semiconductor substrate	2: conductive layer
3: insulating layer	4: antireflection layer
5: plug	6: metal silicide layer
7: barrier metal layer	8: seed layer
9: dummy oxide layer	10: lower electrode
11: dielectric layer	12: upper electrode

【Detailed Description of the Invention】

【Object of the Invention】

【Field of the Invention and the Related Prior Art】

The present invention relates to a method for manufacturing a capacitor including a high dielectric layer; and more particularly, to a method for manufacturing a capacitor having dielectric layer capable of preventing the oxidation of a barrier metal layer and the reduction of

capacitance.

A memory cell in a semiconductor memory device, such as a DRAM (Dynamic Random Access Memory) typically consists of one transistor and one capacitor, in which one bit of data is stored in a cell by using an electric charge.

A capacitor comprises of a lower electrode connected to the junction of the transistor, and the junction and the lower electrode is connected through a contact hole formed in an insulating layer.

As the integration of a semiconductor memory device is increase, size of the device is decreased. Therefore, it is difficult to connect the lower electrode to the junction through a fine contact hole, and misalign is generated in manufacturing processes.

As an example, the lower electrode and a plug formed in a contact hole is misaligned during a photolithography process for forming the lower electrode on the plug, and a barrier metal layer formed on the plug is exposed. The exposed barrier metal layer is oxidized during the process of depositing a high dielectric layer, and the dielectric constant of the high dielectric layer is decreased because of the oxidized barrier metal layer.

In order to prevent the oxidation of the barrier metal layer, a method for forming a dielectric layer in low temperature has been developed, however enough capacitance cannot be obtained yet from the dielectric layer formed in the low temperature.

As the integration of the device increased, the problem of misalign becomes more serious matter, and, therefore, it is needed to develop a new method.

Instead of a stack capacitor, a concave capacitor is developed in order to prevent misalign. However, in the highly integrated device in which the area for capacitor is reduced, the concave capacitor is formed more highly than the stack capacitor. Accordingly, the process margin is reduced and the difficulties of fabricating are increased.

An electroplating has been introduced as a new method, in the electroplating, a blanket etch is needed to separate adjacent lower electrodes after depositing a conductive layer on a seed layer. However, the misalign also arises in the blanket etch, the conductive layer is damaged, and the misalign cannot be prevented.

【Preferred Embodiments of the Invention】

It is, therefore, an object of the present invention to provide a method of fabricating a high dielectric capacitor preventing the misalign. In the present invention, a portion of a plug in the contact hole is removed, a metal silicide, a barrier metal layer and a seed layer are stacked on the plug, and then, a lower electrode is formed on the seed layer, in order to prevent the misalign.

【Description of the Invention】

In accordance with an aspect of the present invention,

there is provided a method for fabricating a high dielectric capacitor, comprising the steps of: forming an insulating layer and an antireflection layer over a semiconductor substrate on which a conductive layer is formed; forming a first contact hole by patterning the antireflection layer and the insulating layer, and forming a plug in the contact hole; removing a portion of the plug, forming a metal silicide and a barrier metal layer on the remaining plug; removing a portion of the barrier metal layer in the contact hole and forming a seed layer on the remaining seed layer; forming a dummy oxide layer over the semiconductor substrate, pattering the dummy oxide layer to form a second contact hole exposing the seed layer in the contact hole, and forming a lower electrode in the second contact hole; and removing the dummy oxide layer and forming a dielectric layer and an upper electrode.

Hereinafter, an embodiment of the present invention will be described in detail referring to the accompanying drawings.

Figs. 1 to 9 are cross sectional view showing a method for fabricating a semiconductor memory device according to an embodiment of the present invention.

As shown in Fig. 1, an insulating layer 3 is formed over a semiconductor substrate 1, on which a conductive layer 2 is formed, and an antireflection layer 4 is formed to a thickness of 300 to 1000 Å on the insulating layer. A doped polysilicon layer is deposited and a thermal treatment

process is performed to activate impurities in the doped polysilicon layer, whereby the conducting layer 2 is formed. The insulating layer 3 is formed with an silicon oxide layer, and the antireflection layer 4 is formed with a silicon nitride layer(SiON) of which etch selectivity is higher than the silicon oxide layer.

As shown in Fig. 2, the antireflection layer 4 and the insulating layer 3 are patterned to form a first contact hole exposing the conducting layer 2, and a plug 5 is formed in the first contact hole. A polysilicon layer is deposited to a thickness of 500 - 3000 Å by a chemical vapor deposition and etched in order to form the plug 5.

Thereafter, as sown in FIG. 3, an etching process is performed to remove the plug 5 by a thickness of 500 to 1500 Å, and a metal layer, such as Ti layer, is formed to a thickness of 100 - 300 Å. For forming the metal silicide on the plug 5, an annealing process is performed, and a wet etching process is performed to remove the metal remaining without forming the silicide. Thereafter, a barrier metal layer 7 is formed on a resulting structure and a planarization process is performed to leave the barrier metal layer 7 only on the silicide layer in the first contact hole. In the above mentioned processes, the annealing is performed by the rapid thermal process(RTP), and the planarization process is performed by the chemical & mechanical polishing(CMP). In addition, the barrier metal layer 7 is formed with TiN or triatomic layer, such as TiSiN, TiAlN,

TaSiN and TaAlN, deposited with a physical vapor deposition(PVD) or a chemical vapor deposition(CVD).

As shown in Fig. 4, the barrier metal layer 7 in the first contact hole is etched with an etchant gas, such as CF_4, having high etch selectivity to the antireflection layer.

As shown in Fig. 5, a seed metal layer 8 is deposited to fill the first contact hole using CVD. The seed metal layer 8 is formed with noble metal, such as Ru, Pt, Ir, SrO, W, Mo, Co, Ni, Au and Ag.

As shown in Fig. 6, a planarization process is performed to leave the seed metal layer 8 only on the barrier metal layer in the first contact hole. The planarization process is performed with CMP or etch back.

As shown in Fig, 7, a dummy oxide 9 is formed to a thickness of 5000 to 10000 Å and selectively etched to form a second contact hole opening exposing the seed metal layer 8, and a lower electrode 10 is formed on the seed metal layer 8 in the opening. In the preferred embodiment of the present invention, a Pt layer as the lower electrode 8, is deposited to a thickness of 3000 - 10000 Å by the electroplating. A current density of 0.1 - 10 mA/cm^2 is imposed on the conducting layer 2 formed on the edge of the semiconductor device 1. On the other hand, the semiconductor substrate 30 may be used as an electrode during the electro plating in case the conducting layer 31 is not formed.

As shown in Fig. 8, the dummy oxide layer 9 is removed

by a wet etching using an HF solution or BOE solution.

As shown in Fig. 9, a dielectric layer 11 and an upper electrode 12 are deposited in order on a resulting structure. In the preferred embodiment of the present invention, a BST layer is deposited to a thickness of 150 - 500 Å at a temperature of 400 - 600 °C for forming the dielectric layer 11, and an annealing for crystallizing the dielectric layer 11 is performed in an N_2 gas atmosphere at a temperature of 500 - 700 °C for 30 - 180 seconds, thereby dielectric characteristic of the dielectric layer 11 may be improved. The upper electrode 12 is formed with a material, such as Pt, Ru, Ir or SrO.

【Effect of the Invention】

As mentioned above, it is possible to prevent the diffusion barrier from being exposed even if the mask misalign is occurred, because the silicide layer, the barrier metal layer and the seed metal layer are formed on the plug, of which a portion is removed, in the contact hole. Accordingly, a sufficient capacitance can be guaranteed and the reliability and the yield of devices can be improved, because the annealing for crystallizing the dielectric layer may be performed at a high temperature

In addition, an excellent high dielectric capacitance can be obtained in devices having 0.1 ㎛ design rule by forming stacked Pt electrode according to the present invention.

【Claims】

【Claim 1】 A method for fabricating a high dielectric capacitor, comprising the steps of:

forming an insulating layer and an antireflection layer over a semiconductor substrate on which a conductive layer is formed;

forming a first contact hole by patterning the antireflection layer and the insulating layer, and forming a plug in the contact hole;

removing a portion of the plug, forming a metal silicide and a barrier metal layer on the remaining plug;

removing a portion of the barrier metal layer in the contact hole and forming a seed layer on the remaining seed layer;

forming a dummy oxide layer over the semiconductor substrate, pattering the dummy oxide layer to form a second contact hole exposing the seed layer in the contact hole, and forming a lower electrode in the second contact hole; and

removing the dummy oxide layer and forming a dielectric layer and an upper electrode.

【Claim 2】 The method as recited in claim 1, wherein the conductive layer is formed with a doped polysilicon layer.

【Claim 3】 The method as recited in claim 1, wherein the

insulating layer is formed with a silicon oxide layer, and wherein the antireflection layer is formed with a silicon nitride layer.

【Claim 4】 The method as recited in claim 1, wherein the plug is formed of doped polysilicon.

【Claim 5】 The method as recited in claim 1, wherein the metal silicide is formed by depositing and annealing a metal layer, and removing the metal layer remaining without reaction.

【Claim 6】 The method as recited in claim 5, wherein the metal layer is formed with Ti.

【Claim 7】 The method as recited in claim 1, wherein the barrier metal layer is formed with TiN, TiSiN, TiAlN TaSiN or TaAlN.

【Claim 8】 The method as recited in claim 1, wherein the seed layer is formed with Ru, Pt, Ir, Pt, SrO, W, Mo, Co, Ni, Au or Ag.

【Claim 9】 The method as recited in claim 1, wherein the dummy oxide layer is formed to a thickness of about 5000 to 10000 Å.

【Claim 10】 The method as recited in claim 1, wherein the lower electrode is formed with Pt using an electroplating.

【Claim 11】 The method as recited in claim 1, wherein the dummy oxide is removed with an HF solution or a BOE.

【Claim 12】 The method as recited in claim 1, wherein the dielectric layer is formed with a BST layer deposited at a temperature of 400 to 600 ℃, wherein the BST layer is deposited to a thickness of 150 to 500 Å, and wherein the BST layer is undergone a rapid thermal process at a temperature of 500 to 700 ℃ in an ambient of nitrogen for 30 to 180 seconds.

【Claim 13】 The method as recited in claim 1, wherein the upper electrode is formed by depositing Pt, Ru or SrO by a chemical vapor deposition.

FIG. 1

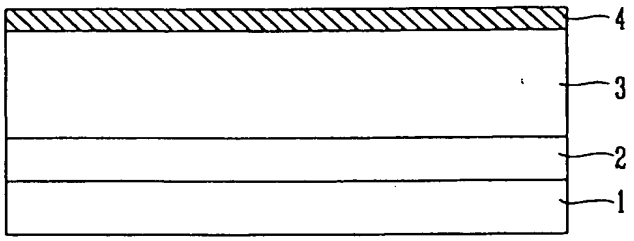

Fig. 2

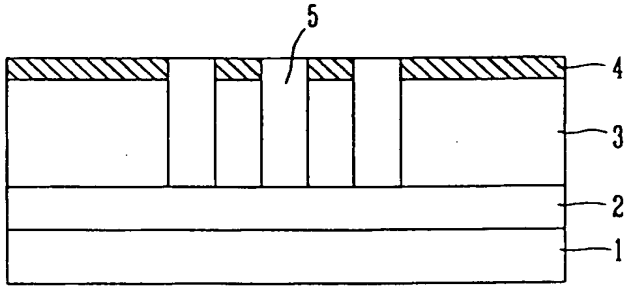

FIG. 3

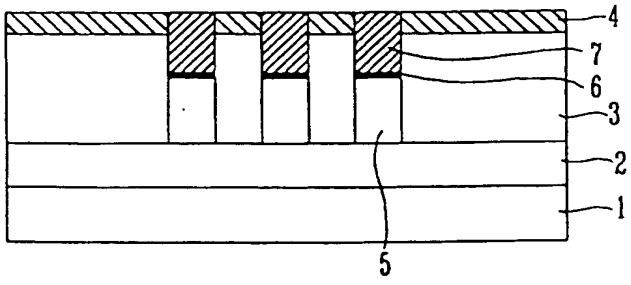

FIG. 4

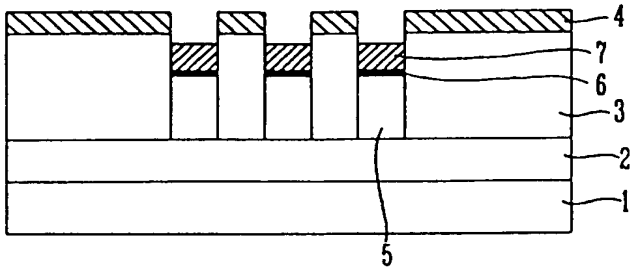

FIG. 5

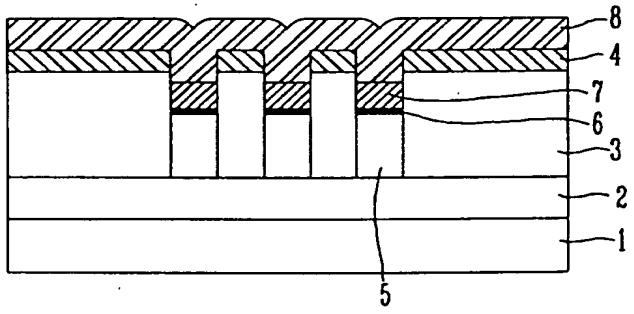

FIG. 6

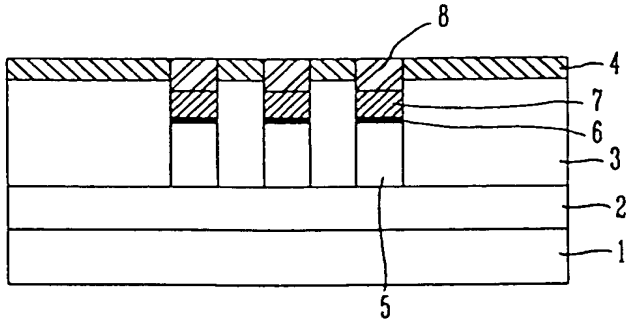

FIG. 7

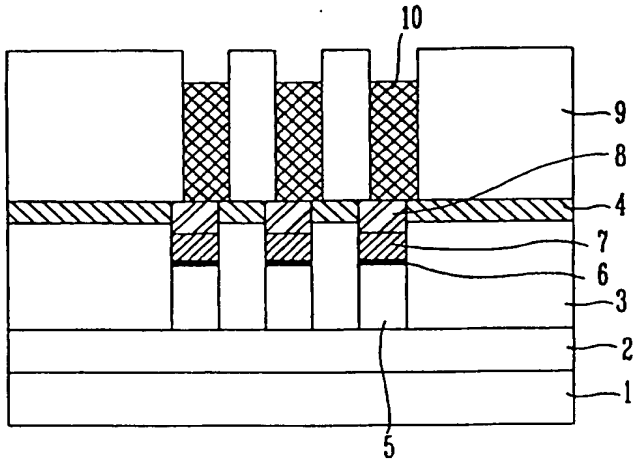

FIG. 8

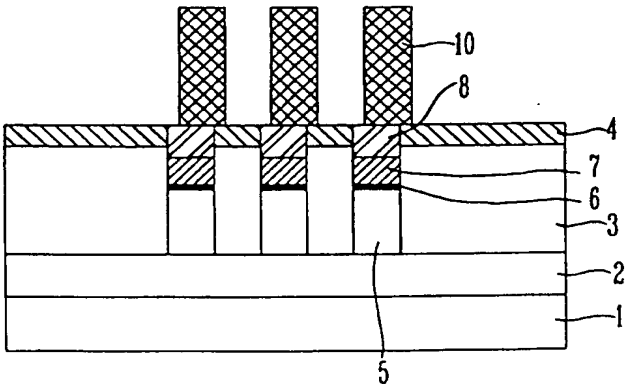

FIG. 9